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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,806	03/30/2004	Siva G. Narendra	INTEL-0038	2840
34610	7590	04/23/2007	EXAMINER	
KED & ASSOCIATES, LLP			BOATENG, ALEXIS ASIEDUA	
P.O. Box 221200			ART UNIT	PAPER NUMBER
Chantilly, VA 20153-1200				2838
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		04/23/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/811,806	NARENDRA ET AL.
	Examiner Alexis Boateng	Art Unit 2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 05 February 2007.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-7, 9-14, 16 - 18, 20, 25, 27 - 35 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-7, 9-14, 16 - 18, 20, 25, 27 - 35 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) Notice of Informal Patent Application
- 6) Other: \_\_\_\_\_

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 – 5, 10, 14, 16, 18, 20, 29 – 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desprez (U.S. 2003/0020435) in view of Rajashekara (U.S. 2005/0047039).

**Regarding claims 1, 2, 3, 14 and 16,** Desprez discloses wherein a system comprising:

a detector to detect a voltage stored in ultra-capacitor (figure 2 item 14; paragraph [0045]);

an extractor to extract energy from the ultra-capacitor (paragraphs [0009] – [0011]). Desprez discloses the invention as previously disclosed, but does not disclose the remainder. Rajashekara discloses in paragraphs [0022] – [0026] and claim 5 wherein the extractor including:

a first amplifier circuit to amplify an output voltage from the ultracapacitor when the detected voltage falls below a first predetermined voltage of a load coupled to the ultracapacitor, the first amplifier circuit to amplify said output voltage independent of a charging operation of the ultracapacitor. At the time of invention, it would have been

obvious to a person of ordinary skill in the art to modify the Desprez system with the Rajashekara system so that it may properly boost the voltage when needed.

**Regarding claims 4,** Desprez discloses wherein a controller to monitor a change in the increased voltage (paragraph [0024] – [0025]), wherein the linear regulator adjusts the changed voltage when the monitored voltage falls below the a predetermined voltage of the load (paragraph [0018]). Desprez discloses the invention as previously claimed, but does not disclose the reminder. Rajashekara discloses a first predetermined level in paragraph [0019], wherein the voltage is boosted to a certain level. These different switches all provide first, second and third levels as disclosed in claim 5. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Desprez system with the Rajashekara system so that the different levels in the system may be met.

**Regarding claims 5 and 18,** Desprez discloses wherein the controller generates a control signal to modify the resistance along the feedback path of the first amplifier circuit to maintain the output voltage of the ultracapaciotr substantially equal to or above the first predetermined voltage of the load (paragraph [0050] – [0054]).

**Regarding claims 10 and 20,** Desprez discloses wherein the extractor includes an adiabatic amplifier to amplify voltage output from the ultracapacitor by a predetermined factor (figure 1 item 12; paragraph [0050]): discloses a bypass circuit, which is a MOSFET. Page 27 of applicant's specification discloses wherein the term adiabatic refers to without generating a "substantial amount of heat." Substantial is a term of degree not defined by specification).

**Regarding claims 29 – 33,** Desprez discloses wherein the first and second predetermined voltages corresponds to a minimum operating voltage of the load and the amplifier circuit (paragraphs [0020] – [0025]).

**Regarding claim 34,** Desprez discloses wherein the extractor is disabled when the detected voltage of the ultracapacitor falls below a second predetermined voltage of the first amplifier circuit (paragraph [0011]).

3. Claims 6, 12, 17, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desprez (U.S. 2003/0020435) in view of Sasaki (U.S. 6,476,587).

**Regarding claim 6,** Desprez does not disclose the invention as claimed. Sasaki discloses in figure 1 item 22 and column 6 lines 15 - 47 wherein a second amplifier is used is to amplify the voltage from the first amplifier. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Desprez system with the Sasaki system so that the load receives the proper amount of voltage.

**Regarding claim 12,** Desprez does not disclose the invention as claimed. Sasaki discloses in figure 1 item 25 works as a transmission gate. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Desprez system with the Sasaki system to that the voltage in the ultracapacitor may be redirected as necessary to the load or through the regulation.

**Regarding claim 17,** Desprez does not disclose the invention as claimed.

Sasaki discloses in figure 2 and column 7 lines 28 – column 8 lines 47 wherein the reduction of the voltage is detected and adjusted to maintain at least the load operating voltage. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Desprez system with the Sasaki system so that the system is not damaged by a too low voltage.

**Regarding claim 35,** Desprez does not disclose the invention as claimed.

Sasaki discloses in column 2 lines 63 – column 3 line 24 wherein the load is connected to path when it is above the first predetermined voltage level and disconnected when its below the first predetermined voltage level. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Desprez system with the Sasaki system so that proper charging is ensured and the system is not damaged by overdischarging.

4. Claims 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desprez (U.S. 2003/0020435) in view of Bhomik (U.S. 6,268,666).

**Regarding claims 7,** Desprez discloses wherein a system comprising:

a detector to detect a voltage stored in ultra-capacitor (figure 2 item 14; paragraph [0045]);  
an extractor to extract energy from the ultra-capacitor (paragraphs [0009] – [0011]). Desprez discloses the invention as previously disclosed, but does not disclose the remainder. Desprez does not disclose the invention as claimed.

Bhomik discloses in column 6 lines 44 – 62 wherein the extractor includes a capacitor voltage increase output from the ultracapacitor. Bhomik further discloses in figure 1A wherein there is a first capacitor, item 80 which is coupled to the ultracapacitor and a second capacitor, item 100, coupled to the ultracapacitor. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Desprez with the Bhomik system so that the system is not damaged by a voltage that is too high or too low.

**Regarding claims 13,** Desprez does not disclose the invention as claimed.

Bhomik discloses in column 1 lines 62 – column 2 lines 7 and column 2 lines 37 – 58 wherein the conversion is a DC-DC step up conversion that steps up the voltage more than two times its amount. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Desprez system with the Bhomik system so that the devices or system is not damaged by incorrect voltage.

5. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desprez (U.S. 2003/0020435) in view of Williams (U.S. 5,517,379).

**Regarding claims 9 and 11,** Desprez does not disclose the invention as claimed. Williams discloses in column 3 lines 51 – 67 wherein a controller is used to monitor the voltage and in column 3 lines 33 – 42 a voltage regulator is used to maintain the voltage. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Desprez system the

Williams system so that the system does not become damaged by incorrect voltage.

- 27k*
3. Claims 25, ~~28~~ are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki (U.S. 6,476,587) in view of Rajashekara (U.S. 2005/0047039).

**Regarding claim 25,** Sasaki disclose wherein a system comprising:

a load (figure 2 item L);  
an ultracapacitor storing a voltage to drive the load (figure 2 item 30);  
an extractor to extract energy from the ultracapacitor when the voltage falls below a predetermined value (figure 2 item 20; column 6 lines 15 - 47). Sasaki discloses the invention as previously disclosed, but does not disclose the remainder. Rajashekara discloses in paragraphs [0022] – [0026] and claim 5 wherein the extractor including:

a first amplifier circuit to amplify an output voltage from the ultracapacitor when the detected voltage falls below a first predetermined voltage of a load coupled to the ultracapacitor, the first amplifier circuit to amplify said output voltage independent of a charging operation of the ultracapacitor. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Sasaki system with the Rajashekara system so that it may properly boost the voltage when needed.

**Regarding claim 27,** Sasaki discloses wherein the load is at least one of a power supply, processor, cache, chipset and a memory (figure 3 shows wherein the

system is used to charge the components of a mobile device which includes a power supply, processor, cache, chipset and memory).

**Regarding claim 28,** Sasaki discloses wherein the load, ultracapacitor and extractor are included on a single die (figure 2).

### ***Response to Arguments***

4. Applicant's arguments with respect to claims 1, 2, 5, 7, 14, 16 and 25 have been considered but are moot in view of the new ground(s) of rejection.
5. Applicant's arguments filed 2/05/07 have been fully considered but they are not persuasive. **Regarding claims 29 and 34,** the applicant argues wherein the features are not taught by the cited references. Desprez discloses in paragraphs [0020] – [0025] wherein the predetermined voltage level corresponds to a minimum operating voltage of the load. **Regarding claim 35,** the applicant argues wherein the features disclosed are not taught or suggested by the cited references. Sasaki discloses in column 2 lines 63 – column 3 line 24 wherein the load is connected to path when it is above the first predetermined voltage level and disconnected when its below the first predetermined voltage level.

### ***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP

Art Unit: 2838

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexis Boateng whose telephone number is (571) 272-5979. The examiner can normally be reached on 8:30 am - 6:00 pm, Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl Easthom can be reached on (571) 272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AB

  
Adolf Berlaine  
Primary Examiner